AMENDMENTS

In the Specification:

Please replace the specification with the attached Substitute Specification.

In the Claims:

Please amend the claims as follows.

1. (Amended) A circuit including an integrated circuit, comprising:

a first switching element coupled to a first terminal and a second terminal;

a second switching element coupled to the first terminal; and

a capacitor coupled between the second switching element and a ground or reference voltage.

2. (Amended) The circuit including an integrated circuit of claim 1, further comprising:

a first clock signal to switch the first switching element between high and low; and

a second clock signal to switch the second switching element between high and low.

3. (Amended) The circuit including an integrated circuit of claim 2, wherein the second clock signal is the phase-shifted complementary signal of the first clock signal.

4. (Amended) The circuit including an integrated circuit of claim 1, wherein

the first terminal is connected to an input of an amplifier that exhibits a high impedance,

the second terminal is connected to an output of a signal source that exhibits a low impedance, and

the circuit operates to substantially null and cancel the charge injection and clock feed-through error voltage, respectively, which occurs when the first switching element at the first terminal is switched off, by absorbing the charge injection into the capacitor and by generating a compensation signal.

5. (Amended) The circuit including an integrated circuit of claim 4, wherein the circuit replaces a switching element in a switched network.

9. (Amended) The switching element of claim 8, wherein the another switching element is connected to a node in the switched network where a charge injection or a clock feed-through error voltage, caused by the switching off of the first switching element, is high.

12. (Amended) A method of nulling a charge, comprising:

switching a first switching element to off by turning a first clock signal to low, injecting a clock feed-through error voltage and stored channel charges in the form of charge injection into a first terminal, which is connected to an input of an amplifier that exhibits a high impedance; and

switching a second switching element to on by turning a second clock signal to high, nulling the injected clock feed-through error voltage and charge injection as a result of the opposite signal polarities and absorbing the charge injection into a capacitor, respectively.

13. (Amended) A method of nulling a charge injection in a switched network, comprising:

injecting a terminal, which is connected to an input of an amplifier that exhibits a high impedance, with a stored channel charge and clock feed-through voltage, which occurs when a first switching element is switched off; and

nulling the charge and voltage injected into the terminal by absorbing the charge in a capacitor and canceling the voltage by a compensation signal with opposite polarity.

14. (Amended) The method of claim 13, wherein

the injecting occurs at a first terminal which is connected to the input of the amplifier at a location exhibiting the high impedance, as a result of providing a first clock signal to a first switch such that the first switch is turned off, and

the nulling occurs as a result of providing a second clock signal to a second switch such that the second switch is turned on, resulting in the compensation signal.

15. (Amended) A circuit including an integrated circuit, comprising:

a first switching element coupled to a first node and a second node;

a second switching element coupled to the first node;

a third switching element coupled to the second node;

a first capacitor coupled between the second switching element and a ground or reference voltage; and

a second capacitor coupled between the third switching element and the ground or reference voltage.

16. (Amended) The circuit including an integrated circuit of claim 15, further comprising:

a first clock signal to switch the first switching element between high and low; and

a second clock signal to switch the second and third switching elements between high and low.

17. (Amended) The circuit including an integrated circuit of claim 16, wherein the second clock signal is the phase-shifted complementary signal of the first clock signal.

18. (Amended) The circuit including an integrated circuit of claim 15, wherein

the first node is connected to an input of an amplifier that exhibits a high impedance,

the second node is connected to the input of the amplifier that exhibits the high impedance,

the circuit operates to substantially null and cancel the charge injection and clock feed-through error voltage, respectively, which are caused by the switching off of the first switching element between the first and second nodes, by absorbing the charge injection into the first and second capacitors and by generating a compensation signal on the first and second nodes.

19. (Amended) The circuit including an integrated circuit of claim 18, wherein the circuit replaces a switching element in a switched network.

20. (Amended) A switching element, comprising:

a circuit including a first switching element coupled to a first node, which is connected to input of an amplifier that exhibits a high impedance, and a second node, which is connected to the input of the amplifier that exhibits the high impedance, a second switching element coupled to the first node, a third switching element coupled to the second node, and a first capacitor coupled between the second switching element and a ground or reference voltage, and a second capacitor coupled between the third switching element and the ground or reference voltage.

21. (Amended) The switching element of claim 20, wherein the circuit substantially nulls a charge injection, when the first switching element between the first and second nodes is switched off, by absorbing the charge injection into the first and second capacitors and canceling the feed-through error voltage, when the first switching element between the first and second nodes is switched off, by generating a compensation signal with opposite polarity at the first and second nodes.

22. (Amended) The switching element of claim 21, wherein the circuit replaces another switching element in a switched network.

23. (Amended) The switching element of claim 22, wherein the another switching element is connected to a node in the switched network where a charge injection or a clock feed-through error voltage, caused by the switching off of the first switching element, is high.

26. (Amended) A method of nulling a charge, comprising:

switching a first switching element to off by turning a first clock signal to low, injecting a clock feed-through error voltage and a stored channel charges as charge injection into a first node, which is connected to an input of an amplifier that exhibits a high impedance and a second node, which is connected to the input of the amplifier that exhibits the high impedance; and

switching a second switching element and a third switching element to on by turning a second clock signal to high, nulling the injected clock feed-through error voltage and charge injection as a result of the opposite signal polarities and absorbing the charge injection into a first capacitor and a second capacitor.

27. (Amended) A method of nulling a charge injection in a switched network, comprising:

injecting a first node, which is connected to an input of an amplifier that exhibits a high impedance, and a second node, which is connected to the input of the amplifier that exhibits the high impedance, with a stored channel charge and clock feed-through voltage, which occurs when the first switching element is switched off; and

nulling the charge and voltage injected into the first and second nodes by absorbing the charge in a first capacitor and a second capacitor and canceling the voltage by a compensation signal with opposite polarity on the first and second nodes.

28. (Amended) The method of claim 27, wherein

the injecting occurs at the first and second node which are connected to an input of an amplifier that exhibits a high impedance, as a result of providing a first clock signal to a first switch such that the first switch is turned off, and

the nulling occurs as a result of providing a second clock signal to a second switch and a third switch such that the second and third switches are turned on, resulting in the compensation signal on the first and second nodes.